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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

BONSHOCK, DENNIS G

ART UNIT PAPER NUMBER

2173

DATE MAILED: 04/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/832,997

Applicant(s)

GABBERT ET AL.

Examiner

Dennis G Bonshock

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 February 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Final Rejection

Response to Amendment

1. It is hereby acknowledged that the following papers have been received and placed on record in the file: Response as received on 2-26-04.

2. Claims 1-26 have been examined.

Status of Claims:

3. Claims 1-10 and 13-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaiser et al., Patent # 4,970,664, hereinafter Kaiser.

4. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaiser and Kodosky et al., Patent #5,301,301, hereinafter Kodosky.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-10 and 13-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaiser et al., Patent # 4,970,664, hereinafter Kaiser.

7. With regard to claim 1, teaching a method for creating a graphical program including a plurality of portions of graphical source code to be executed sequentially, Kaiser teaches, in column 1, lines 30-42 and column 6, lines 11-17, a program consisting of graphical sources code which is executed sequentially. With regard to claim 1, further teaching displaying a plurality of frames in the graphical program such

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that two or more frames are visible at the same time, Kaiser teaches, in column 2, lines 20-24 and in figure 2, two or more frames visible together. With regard to claim 1, further teaching including a portion of graphical source code in each frame in response to user input, Kaiser teaches, in column 3, lines 60-66, the user entering graphical source code into the environment via a schematic editor. With regard to claim 1, further teaching the plurality of frames defining an execution order for the plurality of portions of graphical source code such that during execution of the graphical program the plurality of portions of graphical source code are executed sequentially, Kaiser teaches, in column 2, lines 20-24, the execution path of the frames being set up, and in column 1, lines 30-42, the sequential execution of the simulated circuit.

8. With regard to claims 2, 15, and 22, which teach a plurality of frames being displayed in the graphical program such that each frame is visible at the same time, Kaiser teaches, in column 2, lines 20-24 and in figure 2, a signal path having portions that appear on separate schematic sheets.

9. With regards to claims 3, 16, and 23, which teach receiving user input indicating a desire to specify a plurality of portions of graphical source code to be executed sequentially, wherein displaying the plurality of frames in the graphical program is performed in response to receiving the user input indicating the desire to specify a plurality of portions of graphical source code to be executed sequentially, Kaiser teaches, in column 4, lines 39-61 and in figure 2, the user selecting schematic sheets to be added sequentially to the circuit and them being displayed on the screen.

10. With regard to claims 4, 17, and 24, which teach the plurality of frames comprised in a sequence structure, wherein displaying the plurality of frames in the graphical program is performed in response to user input indicating a desire to include a sequence structure in the graphical program, Kaiser teaches, in column 4, lines 39-61 and in figure 2, a plurality of frames that are formed into a sequence structure baring user selection of screens.

11. With regard to claims 5, 18, and 25, which teach each frame being displayed side by side in a left-to-right order, wherein the plurality of frames define an execution order for the plurality of portions of graphical source code such that during execution of the graphical program the plurality of portions of graphical source code are executed sequentially in the left-to-right order, Kaiser teaches, in column 1, lines 30-42, column 4, line 34 through column 5, line 29, and figure 2, a group of screens containing circuit elements connected to one another horizontally in which they are executed in a sequential order.

12. With regard to claims 6 and 19, which teach executing the graphical program, wherein executing comprises executing each portion of graphical source code sequentially according to the execution order defined by the plurality of frames, Kaiser teaches, in column 1, lines 14-42 and column 2, lines 38-40, executing a user arranged group of schematic sheets sequentially.

13. With regard to claim 7, teaching including a portion of graphical source code in the frame in response to user input comprising: including one or more nodes in the frame in response to user input, Kaiser teaches, in column 3, lines 34-43 and lines 60-

66, the schematic editor being capable of adding components to a sheet. With regard to claim 7, further teaching if two or more nodes are included in the frame, interconnecting the two or more nodes in response to user input, Kaiser teaches, in column 3, lines 34-43 and lines 60-66, wire connections between instances (components).

14. With regard to claim 8, teaching displaying a wire in response to user input, Kaiser teaches, in column 3, lines 60-66, a wire connection between instances (components). With regard to claim 8 further teaching defining endpoints for the wire in response to user input, such that a first endpoint of the wire is in a first frame having an associated first portion of graphical source code and a second endpoint of the wire in a second frame having an associated second portion of graphical source code, Kaiser teaches, in column 3, lines 60-66, column 7, lines 33-49, and in figure 2, wire connecting specific net pointes (begin/end points of sheets). With regard to claim 8, further teaching the wire being operable to cause data to be passed from the first portion of graphical source code to the second portion of graphical source code during execution of the graphical program, Kaiser teaches, in column 3, lines 60-66, column 7, lines 33-49, and in figure 2, a wire connecting specific net pointes (begin/end points of sheets) for use in transmitting data between sheets.

15. With regard to claim 9, which teaches including a portion of graphical source code in the graphical program that is not associated with one of the frames, Kaiser teaches, in column 8, lines 21-27, and in figure 2, including "stub net 32" as a access point to the leftmost sheet.

16. With regard to claim 10, which teaches displaying a wire in response to user input, Kaiser teaches, in column 3, lines 60-66, displaying a wire to connect components. With regard to claim 10, further teaching defining end points for the wire in response to user input, such that a first endpoint of the wire is in a first frame having an associated first portion of graphical source code and a second endpoint of the wire is in the portion of graphical source code that is not associated with one of the frames, Kaiser teaches, in column 3, lines 60-66, column 8, lines 21-27, and in figure 2, two endpoints, one in the first sheet and one to the left of the first sheet. With regard to claim 10, further teaching the wire operable to cause data to be passed from the first portion of graphical source code to the portion of graphical source code that is not associated with one of the frames during execution of the graphical program, Kaiser teaches, in column 3, lines 60 through column 4 line 2, column 8, lines 21-27, and in figure 2, the wires which connect sheets being capable of being used by simulators and timing analyzers.

17. With regard to claims 13, 20, and 26, which teach the graphical program being a graphical data-flow program, Kaiser teaches, in column 2, lines 15-23 and column 3, lines 60-66, a program, having graphical representation of source code, in which data flows through circuits.

18. With regard to claim 14, which teaches a graphical program including a plurality of portions of graphical source code to be executed sequentially, Kaiser teaches, in column 1, lines 30-42 and in column 6, lines 11-17, a plurality of portions of graphical source code that are executed sequentially. With regard to claim 14, further teaching

the system comprising a processor and a memory storing program instructions, Kaiser inherently teaches, in column 2, lines 15-23 and column 3, lines 30-43, a computer which contains both a processor and a memory storing program instructions. With regard to claim 14, further teaching displaying a plurality of frames in the graphical program such that two or more frames are visible at the same time, Kaiser teaches, in column 2, lines 20-24 and in figure 2, two or more frames visible together. With regard to claim 14, further teaching including a portion of graphical source code in each frame in response to user input, Kaiser teaches, in column 3, lines 60-66, the user entering graphical source code into the environment via a schematic editor. With regard to claim 14, further teaching the plurality of frames defining an execution order for the plurality of portions of graphical source code such that during execution of the graphical program the plurality of portions of graphical source code are executed sequentially, Kaiser teaches, in column 2, lines 20-24, the execution path of the frames being set up, and in column 1, lines 30-42, the sequential execution of the simulated circuit.

19. With regard to claim 21, which teaches a memory medium for creating a graphical program including a plurality of portions of graphical source code to execute sequentially, Kaiser teaches, in column 1, lines 30-42 and column 6, lines 11-17, a program consisting of graphical sources code, which is executed sequentially. With regard to claim 21, further teaching displaying a plurality of frames in the graphical program such that two or more frames are visible at the same time, Kaiser teaches, in column 2, lines 20-24 and in figure 2, two or more frames visible together. With regard to claim 21, further teaching including a portion of graphical source code in each frame

in response to user input, Kaiser teaches, in column 3, lines 60-66, the user entering graphical source code into the environment via a schematic editor. With regard to claim 21, further teaching the plurality of frames defining an execution order for the plurality of portions of graphical source code such that during execution of the graphical program the plurality of portions of graphical source code are executed sequentially, Kaiser teaches, in column 2, lines 20-24, the execution path of the frames being set up, and in column 1, lines 30-42, the sequential execution of the simulated circuit.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

21. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaiser and Kodosky et al., Patent #5,301,301, hereinafter Kodosky.

22. With regard to claim 11, Kaiser teaches the execution order in which the first frame comes before a second frame having an associated second portion of graphical source code (see column 1, lines 30-42, column 2, lines 20-24, and figure 2). Kaiser however, doesn't teach the data being passed from the first portion to the portion of graphical source code that is not associated with one of the frames without waiting for the second portion of graphical source code to be executed. Kodosky teaches a circuit grouping and execution program similar to that of Kaiser, but further teaches the data being passed from the first portion to the portion of graphical source code that is not

associated with one of the frames without waiting for the second portion of graphical source code to be executed (see figure 3 and column 1, lines 23-43 which show the first portion of graphical source code passing data to both a piece of source code not associated with either frame and also passing it to the second frame). It would have been obvious to one of ordinary skill in the art, having the teachings of Kaiser and Kodosky before him at the time the invention was made to modify the circuit program of Kaiser to include the parallel execution of two independent items as did Kodosky. One would have been motivated to make such a combination because electronic circuits have this functionality, so it would be useful to be able to simulate it.

23. With regard to claim 12, Kaiser teaches a plurality of frames being a first plurality of frames (see column 2, lines 20-24 and figure 2), including graphical source code in the frames (see column 3, lines 60-66), and sequential execution of frames (see column 1, lines 30-42 and column 2, lines 32-40). Kaiser, however, doesn't teach a frame containing another frame of graphical source code, and displaying a frame that contains another frame containing graphical source code. Kodosky teaches a circuit grouping and execution program similar to that of Kaiser, but further teaches that a circuit can contain a frame that contains a second frame with a plurality of graphical source code included (see figure 3 and column 1, lines 23-43). Kodosky further teaches displaying this frame that contains another frame containing graphical source code wherein a plurality of frames are displayed at the same time (see figure 3 and column 1, lines 23-43). It would have been obvious to one of ordinary skill in the art, having the teachings of Kaiser and Kodosky before him at the time the invention was made to modify the

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circuit program of Kaiser to include the ability to embed a frame in another frame as did Kodosky. One would have been motivated to make such a combination because electronic circuits have this functionality so it would be useful to be able to simulate it.

Response to Arguments

24. The arguments filed on 2-26-04 have been fully considered, but they are not persuasive. Reasons are set forth below.

25. With respect to the applicants argument, that Kaiser doesn't teach or suggest "...creating a graphical program including a plurality of portions of graphical source code to be executed sequentially..."

26. In response, the examiner respectfully submits that Kaiser does teaches, column 3, lines 34-44 and lines 60-66, and in column 4, lines 53-56, a path modeling program comprising a plurality of schematic sheets each containing their own executable code, connected to other schematic sheets through the use of wires, where the circuits use sequential logic (see column 1, lines 30-33).

27. With respect to the applicant's argument, that Kaiser doesn't teach a plurality of frames defining an execution order.

28. In response, the examiner respectfully submits that Kaiser does teaches, column 3, lines 34-44 and lines 60-66, and in column 4, lines 53-56, a circuit modeling program comprising a plurality of schematic sheets connected through the use of wires, where the circuits use sequential logic (see column 1, lines 30-33).

29. With respect to the applicant's argument, that there is no reason to combine the teachings of Kaiser with the parallel execution of two independent items and the embedded frames as did Kodosky.

30. In response, the examiner respectfully submits that both Kaiser and Kodosky teach systems which have code represented by figures where figures are partitioned into different frames which are connected thereby defining the execution order (see column 3, lines 34-44 and lines 60-66, and in column 4, lines 53-56 of Kaiser and column 1, lines 54-67 and figure 3 of Kodosky). It is further noted that Kaiser teaches in column 3, lines 34-41, schematic editors which are known in the art to allow for the simulation of parallel paths. With regard to the later response by the applicant that the applicant has not found an electronic circuit containing a frame that contains a second frame with a plurality of graphical source code included, the applicant is again directed to figure 3 of Kodosky where the darker outer frame contains two frames the frame bordered by the page look and the frame with "true" in its upper wall.

Conclusion

31. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

32. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

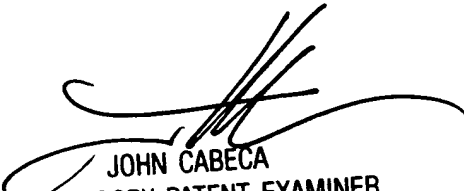
extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis G Bonshock whose telephone number is (703)305-4668. The examiner can normally be reached on Monday - Friday, 8:30 a.m. - 5:00 p.m.

34. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Cabeca can be reached on (703)308-3116. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

35. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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